HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200300183-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Schlankser et al. **Confirmation No.:**

Application No.: **Examiner:**

Filing Date: **Group Art Unit:**

Title: METHOD OF DESIGNING CUSTOM CIRCUIT DEVICE

COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EU687335576US**

Date of Deposit **10/30/2003**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By _____

Typed Name: **Daniel Ratoff**

Respectfully submitted,

Schlankser et al.

By _____

Derek J. Westberg

Attorney/Agent for Applicant(s)
Reg. No. **40,872**

Date: **10/30/2003**

Telephone No.: **(408) 293-9000**

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200300183-1	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT Schlansker et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	1A	6,204,690	Mar. 20, 2001	Young et al.	
	1B	6,243,851	Jun. 5, 2001	Hwang et al.	
	1C	6,292,022	Sep. 18, 2001	Young et al.	
	1D	6,553,395	Apr 22, 2003	Marshall et al.	
	1E	6,353,841	Mar. 5, 2003	Marshall et al.	
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

FOREIGN PATENT DOCUMENTS

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	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	V. Kathail, et al., PICO (Program In, Chip Out) : Automatically Designing Custom Computers, IEEE Computer, September 2002, 35(9), pp. 39-47.
	1R	S. C. Goldstein, et al., PipeRench: A Reconfigurable Architecture and Compiler, IEEE Computer, April 2000, 33(4).
	1S	S. C. Goldstein, et al., PipeRench: A Coprocessor for Streaming Multimedia Acceleration, In Proceedings of the 26th Annual International Symposium on Computer Architecture, 1999, pp. 28-39.

EXAMINER	DATE CONSIDERED

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	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	2Q	V. Betz and J. Rose, Effect of the Prefabricated Routing Track Distribution on FPGA Area-Efficiency, IEEE Transactions on VLSI, Sept. 1998, 6(3), pp. 445-456.
	2R	Emre Özer, Sanjeev Banerjia, and Thomas M. Conte, Unified Assign and Schedule: A New Approach to Scheduling for Clustered Register File Microarchitectures, In Proceedings of the 31th Annual International Symposium on Microarchitecture (MICRO-31), Dallas, Texas, 1998, pp. 308-315.
	2S	M.C. Papaefthymiou, Understanding Retiming Through Maximum Average-Delay Cycles, Mathematical Systems Theory, 1994, 1(27), pp. 65-84.

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	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	3Q	J. Babb, R. Tessier, and A. Agarwal, Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators, In Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines, Los Alamitos, CA 1993, pp. 142-151.
	3R	J.S. Rose and S. Brown, Flexibility of Interconnection Structures for Field-Programmable Gate Arrays, IEEE JSSC, March 1991, 26(3), pp. 277-282.
	3S	S. Note, et al., Cathedral III: Architecture driven high-level synthesis for high throughput DSP applications, In Proceedings of the 28th ACM/IEEE Design Automation Conference, DAC 91, San Francisco, CA, 1991, pp. 597 - 602.

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	4L					
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	4P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	4Q	Constantine N. ANAGNOSTOPOULOS, Paul P. K. LEE, Application-Specific Integrated Circuits, The Electronics Handbook, pp. 731-748, CRC Press, Boca Raton FL, 1996.
	4R	Bradley K. FAWCETT, Software Development Tools for Field Programmable Gate Array Devices, The Electronics Handbook, pp. 784-793, CRC Press, Boca Raton FL, 1996.
	4S	

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